IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Abbott	Art Unit:	2826
Serial No.:	09/525,105	Examiner:	Williams, A
Filed:	03/14/00	Docket:	TI-28098

For: **"SEMICONDUCTOR CIRCUIT ASSEMBLY HAVING A PLATED LEADFRAME INCLUDING GOLD SELECTIVELY COVERING AREAS TO BE SOLDERED"**

REPLACEMENT PAGES

June 28, 2001

Assistant Commissioner
for Patents
Washington, D.C. 20231

MAILING CERTIFICATE UNDER 37 C.F.R.1.8(A)
I hereby certify that the above correspondence is being deposited with the U.S. Postal Service as First Class Mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231 on June 28, 2001.
Glenda West 6/28/01
Glenda West Date

Sir:

As a supplement to the Amendment mailed June 28, 2001, please enter the enclosed replacement pages, including a clean version and a marked-up version.

Respectfully submitted,

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Enclosures

WE CLAIM:

1. A leadframe for use with integrated circuit chips comprising:
a plated layer of gold selectively covering outer areas of said leadframe intended for solder attachment.

2. A leadframe for use with integrated circuit chips, having a chip mount pad and a plurality of lead segments, comprising:
a leadframe base made of copper or copper alloy;
a first layer of nickel deposited on said copper or copper alloy; a layer of an alloy of nickel and palladium on said first nickel layer; a second layer of nickel on said alloy layer, said second nickel layer deposited to be suitable for bending of said lead segments, wire bonding, and solder attachment;
a layer of palladium, said palladium layer deposited to be suitable for protecting the nickel surface for wire bonding and solderability, and for adhesion to molding compound; and a layer of gold selectively covering outer areas of said lead segments intended for solder attachment.

3. The leadframe according to Claim 2 wherein said gold layer has a thickness in the range from 2 to 5 nm.

4. The leadframe according to Claim 2 wherein said first nickel layer has a thickness in the range from 50 to 150 nm.

5. The leadframe according to Claim 2 wherein said alloy layer has a thickness in the range from 50 to 150 nm.

6. The leadframe according to Claim 2 wherein said second nickel layer has a thickness in the range from 1000 to

3000 nm.

7. The leadframe according to Claim 2 wherein said palladium layer has a thickness in the range from 25 to 75 nm.

8. The leadframe according to Claim 2 wherein said copper or copper alloy base has a thickness between about 100 and 250 μm.

9. The leadframe according to Claim 2 wherein said solder attachment comprises solder materials selected from a group consisting of tin/lead, tin/indium, tin/silver, tin/bismuth and conductive adhesive compounds.

10. The leadframe according to Claim 1 wherein said leadframe comprises an iron-nickel alloy or invar base, selectively plated with gold.

11. A semiconductor device comprising:
a leadframe comprising a chip mount pad for an integrated circuit chip and a plurality of lead segments having their first end near said mount pad and their second end remote from said mount pad; said leadframe having a first surface layer of nickel, a layer of an alloy of nickel and palladium, a second layer of nickel, and a layer of palladium; said leadframe further having an outermost layer of gold selectively covering said second ends of said lead segments in a thickness suitable to optimize solder attachment; an integrated circuit chip attached to said mount pad; bonding wires interconnecting said chip and said first ends of said lead segments; encapsulation material surrounding said chip, bonding wires and said first ends of said lead segments, whereby the adhesion between said encapsulation material and said surrounded parts is

maximized; and said encapsulation material leaving said second ends of said lead segments exposed, whereby the solder attachment to said gold layer is maximized.

12. The device according to Claim 11 wherein said bonding wires are selected from a group consisting of gold, copper, aluminum and alloys thereof.

13. The device according to Claim 11 wherein the bonding wire contacts to said first ends of said lead segments comprise welds made by ball bonds, stitch bonds, or wedge bonds.

14. The device according to Claim 11 wherein said encapsulation material is selected from a group consisting of epoxy-based molding compounds suitable for adhesion to said leadframe.

15. The device according to Claim 11 further comprising lead segments having said second ends bent, whereby said segments obtain a form suitable for solder attachment.

16. A method for fabricating a leadframe comprising a chip mount pad and a plurality of lead segments having their first end near said mount pad and their second end remote from said mount pad, comprising the steps of selectively masking said chip pad and said first segment ends, thereby leaving said second segment ends exposed; and plating a layer of gold on said exposed segment ends in a thickness suitable to optimize solder attachment, thereby creating a visual distinction between the gold-plated and unplated leadframe areas.

17. A method for fabricating a leadframe comprising the steps of:

providing a copper leadframe having a mount pad for an integrated circuit chip and a plurality of lead segments having their first end near said mount pad and their second end remote from said mount pad; cleaning said leadframe in alkaline soak cleaning and alkaline electrocleaning; activating said leadframe by immersing said leadframe into an acid solution, thereby dissolving any copper oxide; immersing said leadframe into an electrolytic nickel plating solution and depositing a first layer of nickel onto said copper; electroplating a layer comprising an alloy of nickel and palladium; electroplating a second layer of nickel, thereby adapting said lead segments for mechanical bending; electroplating a layer of palladium; selectively masking said chip pad and said first segment ends, thereby leaving said second segment ends exposed; and plating a layer of gold on said exposed segment ends in a thickness suitable to optimize solder attachment, thereby creating a visual distinction between the gold-plated and unplated leadframe areas.

18. The method according to Claim 17 wherein said gold plating is performed electrolytically or electrolessly.

19. The method according to Claim 17 wherein said masked parts of said leadframe comprise the leadframe areas to be encapsulated by molding compound.

20. The method according to Claim 17 wherein the process steps are executed in sequence without time delays, yet including intermediate rinsing steps.

21. The method according to Claim 17 wherein said acid

solution may be sulfuric acid, hydrochloric acid or any other acid.

22. A method for fabricating a leadframe comprising the steps of:

providing a copper leadframe having a mount pad for an integrated circuit chip and a plurality if lead segments having their first end near said mount pad and their second end remote from said mount pad; cleaning said leadframe in alkaline soak cleaning and alkaline electrocleaning activating said leadframe by immersing said leadframe into an acid solution, thereby dissolving any copper oxide;

electroplating a layer of nickel, thereby adapting said lead segments for mechanical bending;

electroplating a layer of palladium; selectively masking said chip pad and said first segment ends, thereby leaving said second segment ends exposed; and

plating a layer of gold on said exposed segment ends in a thickness suitable to optimize solder attachment, thereby creating a visual distinction between the gold-plated and unplated leadframe.